Customer No.: 31561
Application No.: 10/710,671
Docket NO.: 13085-US-PA

AMENDMENT

Please amend the application as indicated hereafter.

In the Claims :

1. (original) A non-volatile memory structure, comprising:

a substrate;

a plurality of gate structures, disposed on the substrate, wherein each substrate structure comprises, from the substrate, at least a bottom dielectric layer, a charge-trapping layer, an upper dielectric layer, a control gate and a cap layer;

a plurality of select gate structures, wherein each of the select gate structures is disposed on one side of each gate structure respectively such that the gate structures are serially connected together to form a memory cell row, wherein each select gate structure comprises, from the substrate, at least a select gate dielectric layer and a select gate;

a plurality of spacers, disposed between the gate structures and the select gate structures; and

a source/drain region, disposed in the substrate on each side of the memory cell row.

2. (original) The non-volatile memory structure of claim 1, wherein each of the select gate structures completely fills the space between the gate structures.

3. (original) The non-volatile memory structure of claim 1, wherein material constituting the charge-trapping layer comprises silicon nitride.

4. (original) The non-volatile memory structure of claim 1, wherein material constituting the bottom dielectric layer and the upper dielectric layer comprises silicon

oxide.

5. (original) The non-volatile memory structure of claim 1, wherein material constituting the control gate and the select gate comprises polysilicon.

6. (original) The non-volatile memory structure of claim 1, wherein the select gate dielectric layer has a thickness between about 160Å to 170Å.

7. (original) A non-volatile memory structure, comprising:

a gate structure, having at least a bottom dielectric layer, a charge-trapping layer, an upper dielectric layer, a control gate and a cap layer over a substrate;

a select gate, disposed on one side of the gate structure;

a spacer, disposed between the gate structure and the select gate;

a select gate dielectric layer, disposed between the select gate and the substrate;

a source region, disposed in the substrate on one side of the gate structure corresponding to the select gate; and

a drain region, disposed in the substrate adjacent to the select gate.

8. (original) The non-volatile memory structure of claim 1, wherein material constituting the charge-trapping layer comprises silicon nitride.

9. (original) The non-volatile memory structure of claim 1, wherein material constituting the bottom dielectric layer comprises silicon oxide.

10. (original) The non-volatile memory structure of claim 1, wherein material constituting the upper dielectric layer comprises silicon oxide.

Claims 11-18 (canceled)